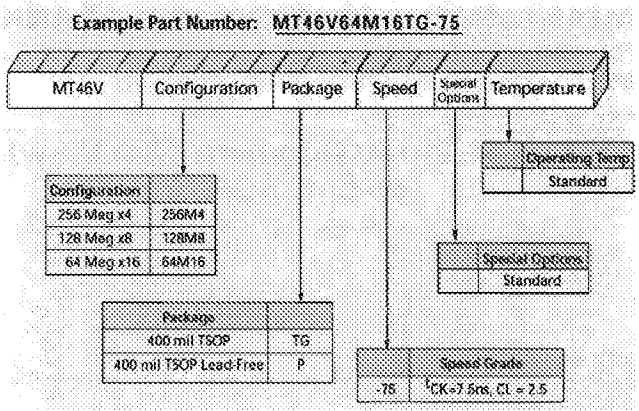
1Gb DDR SDRAM Part Numbers



General Description

The 1Gb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. It is internally configured as a quad-bank DRAM.

The 1Gb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $2n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 1Gb DDR SDRAM effectively consists of a single $2n$-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 1Gb DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL_2. All full drive option outputs are SSTL_2, Class II compatible.

NOTE:
1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
2. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.
3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
4. Any specific requirement takes precedence over a general statement.

DOUBLE DATA RATE (DDR) SDRAM

MT46V256M4 – 64 MEG X 4 X 4 BANKS
MT46V128M8 – 32 MEG X 8 X 4 BANKS
MT46V64M16 – 16 MEG X 16 X 4 BANKS

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/datasheets

Features

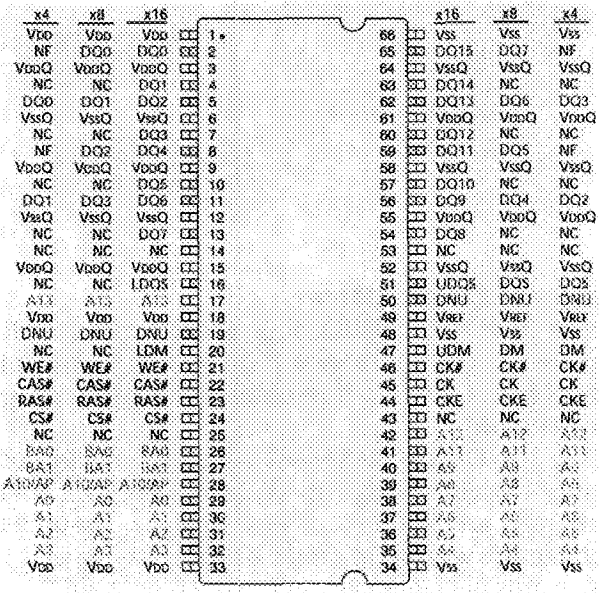
- VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two –one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes
- Longer lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported
- tRAS lockout supported (tRAP = tRCD)

OPTIONS — MARKING

- Configuration
  - 256 Meg x 4 (64 Meg x 4 x 4 banks) — 256M4
  - 128 Meg x 8 (32 Meg x 8 x 4 banks) — 128M8
  - 64 Meg x 16 (16 Meg x 16 x 4 banks) — 64M16
- Plastic Package – OCPL
  - 66-pin TSOP(400 mil width, 0.65mm pin pitch) — TG
  - 66-pin TSOP Lead-Free (400 mil width, 0.65mm pin pitch) — P
- Timing – Cycle Time
  - 7.5ns @ CL = 2.5 (DDR266B)[1, 2] — -75
- Temperature Rating
  - Commercial Temperature (0°C to +70°C) — None

NOTE: 1. Supports PC2100 modules with 2.5-3-3 timing
2. Supports PC1600 modules with 2-2-2 timing.

Figure 1: Pin Assignment (Top View) 66-pin TSOP



	256 MEG X 4	128 MEG X 8	64 MEG X 16
Configuration	64 Meg x 4 x 4 banks	32 Meg x 8 x 4 banks	16 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addressing	16K (A0–A13)	16K (A0–A13)	16K (A0–A13)
Bank Addressing	4(BA0,BA1)	4(BA0,BA1)	4(BA0,BA1)
Column Addressing	4K(A0–A9, A11, A12)	2K(A0–A9, A11)	1K(A0–A9)

Key Timing Parameters

SPEED GRADE	CLOCKRATE CL=2**	CLOCKRATE CL=2.5**	DATA-OUT WINDOW*	ACCESS WINDOW	DQS–DQ SKEW
-75	100 MHz	133MHz	2.5ns	±0.75ns	+0.5ns

* Minimum clock rate @ CL= 2.5
** CL = CAS (Read) Latency

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Figure 2: Functional Block Diagram 256 Meg x4

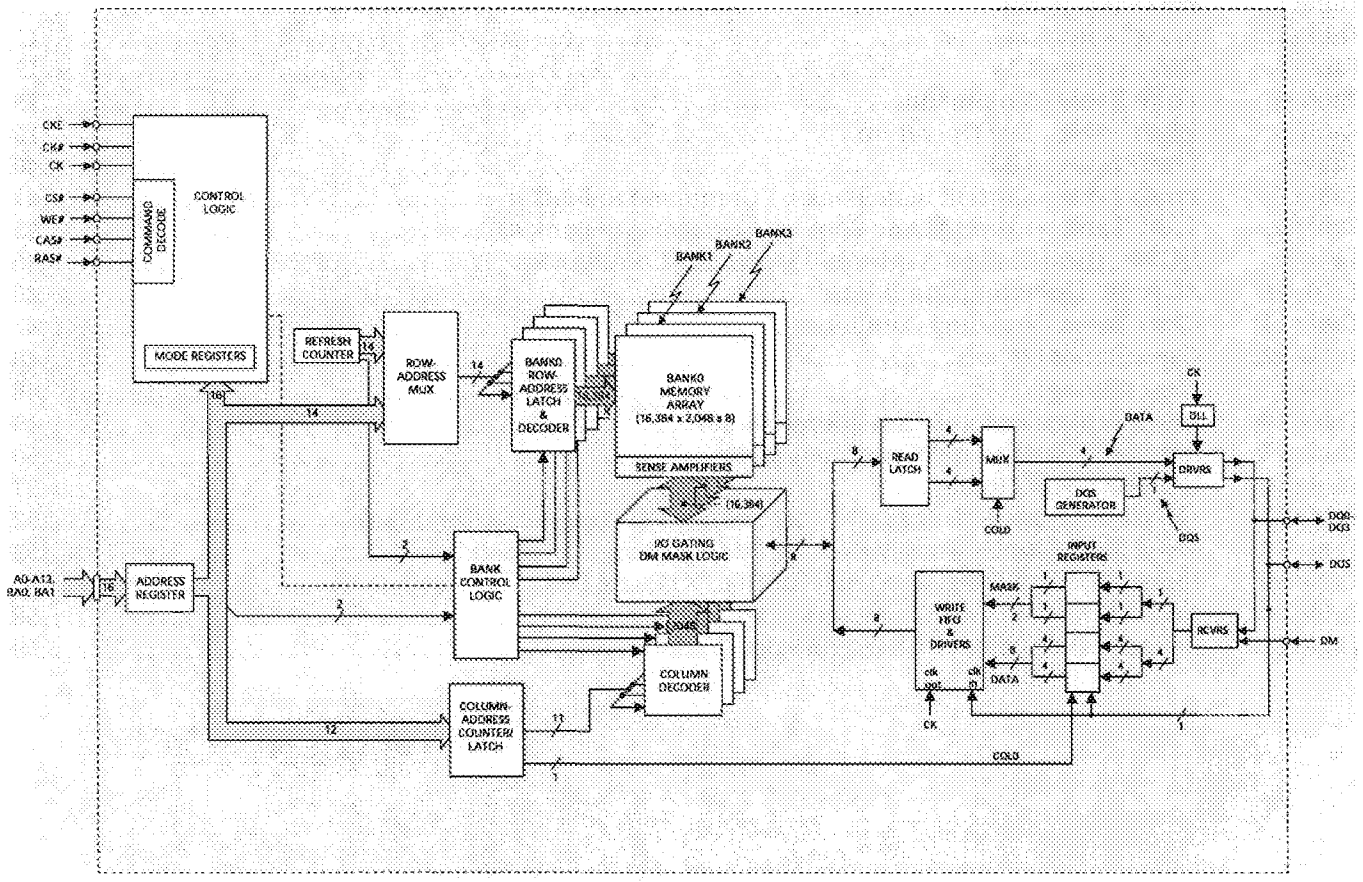

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Figure 4: Functional Block Diagram 64 Meg x16

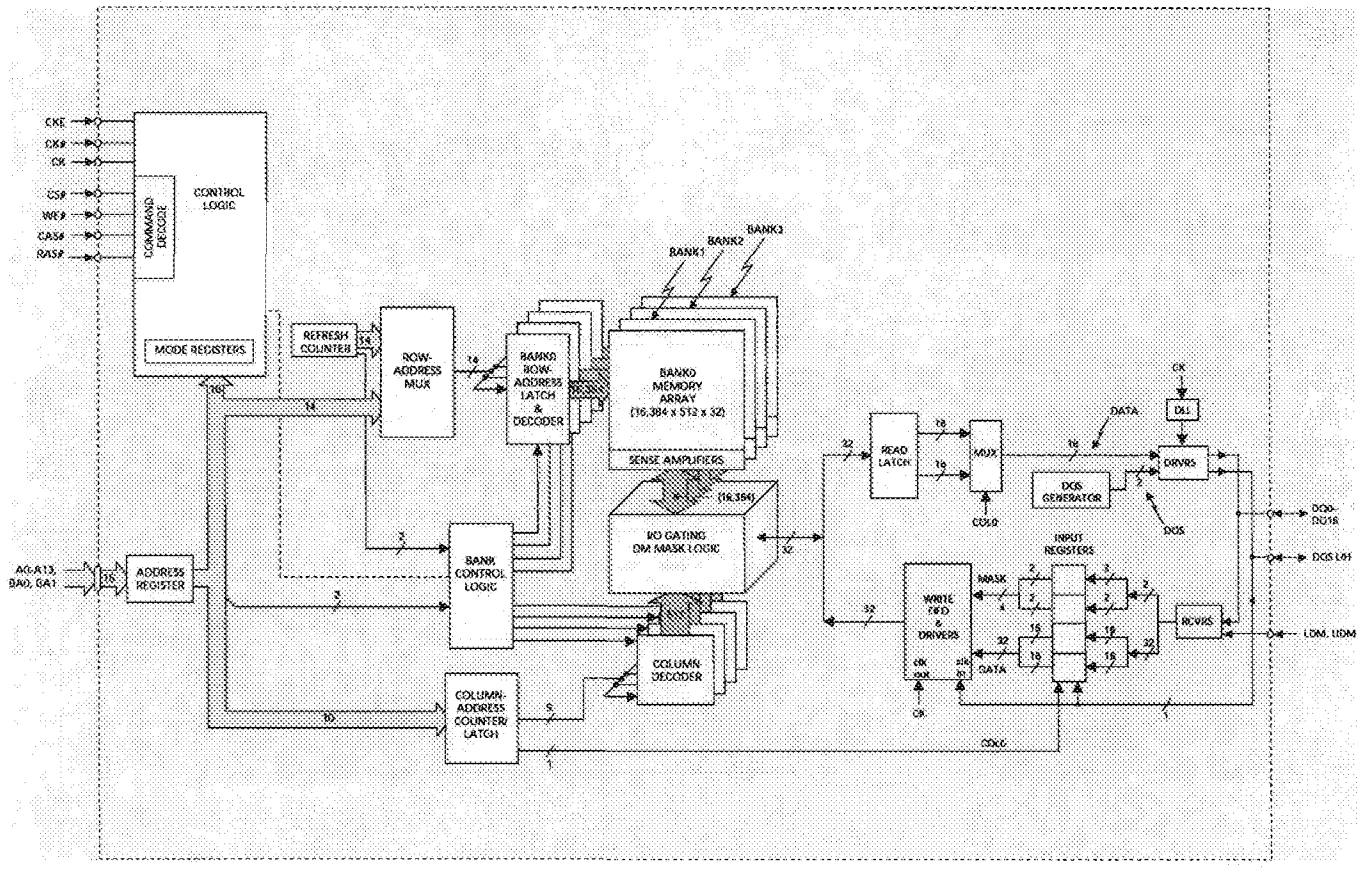


Figure 3: Functional Block Diagram 128 Meg x8

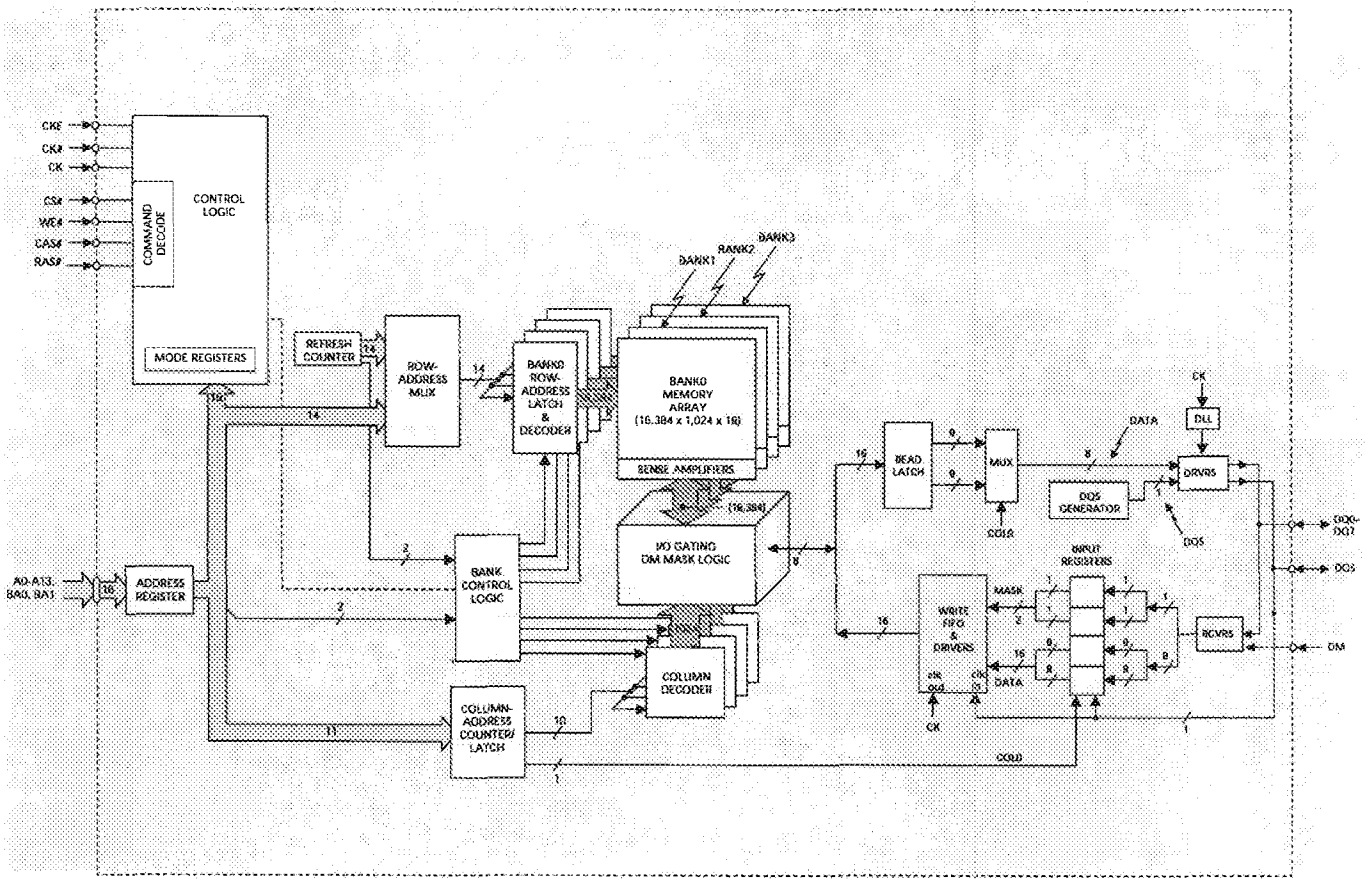


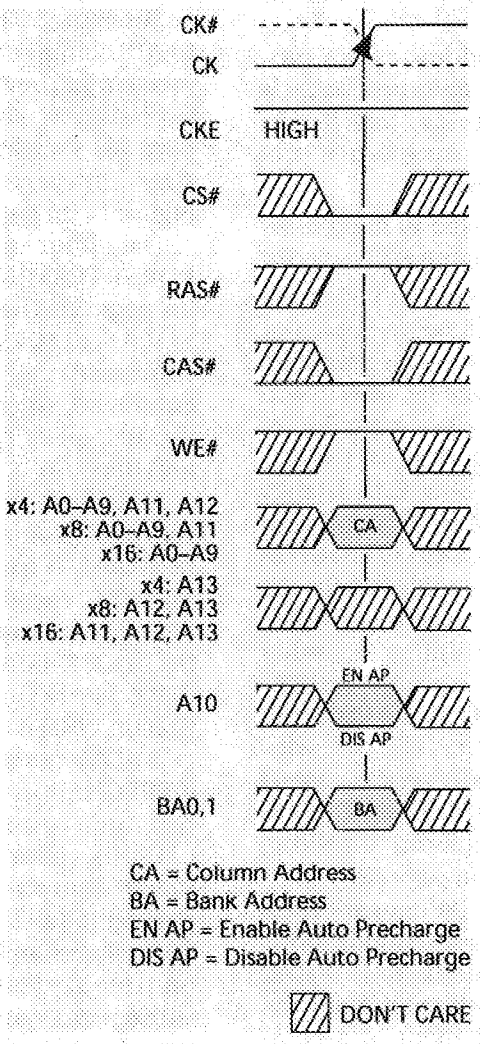
Table 1: Pin Descriptions (Continued)

TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0–DQ2 DQ3–DQ5 DQ6–DQ8 DQ9–DQ11 DQ12–DQ14 DQ15	I/O	Data Input/Output: Data bus for **x16**
14, 25, 43, 53	NC	–	No Connect for **x16** These pins should be left unconnected.
2, 5, 8, 11, 56, 59, 62, 65	DQ0–DQ2 DQ3–DQ5 DQ6, DQ7	I/O	Data Input/Output: Data bus for **x8**
4, 7, 10, 13, 14, 16, 20, 25, 43, 53, 54, 57, 60, 63,	NC	–	No Connect for **x8** These pins should be left unconnected.
5, 11, 56, 62	DQ0–DQ2 DQ3	I/O	Data Input/Output: Data bus for **x4**
4, 7, 10, 13, 14, 16, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	No Connect for **x4** These pins should be left unconnected.
2, 8, 59, 65	NF	–	No Function for **x4** These pins should be left unconnected.
51 16 51	DQS LDQS UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 (E7) is NC on x4 and x8.
19, 50	DNU	–	Do Not Use: Must float to minimize noise on V_{REF}.
3, 9, 15, 55, 61	$V_{DD}Q$	Supply	DQ Power Supply: +2.5V ±0.2V. Isolated on the die for improved noise immunity.
6, 12, 52, 58, 64	$V_{SS}Q$	Supply	DQ Ground. Isolated on the die for improved noise immunity.
1, 18, 33	V_{DD}	Supply	Power Supply: +2.5V ±0.2V.
34, 48, 66	V_{SS}	Supply	Ground.
49	V_{REF}	Supply	SSTL_2 reference voltage.

Table 1: Pin Descriptions

TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER- DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
47 20, 47	DM LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15. Pin 20 is a NC on x4 and x8.
26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 28, 41, 42, 17	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.

Figure 10: READ Command



READs

READ bursts are initiated with a READ command, as shown in Figure 10 on page 20.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

NOTE: For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 11 on page 21 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 38 on page 60 and Figure 39 on page 61. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is depicted in Figure 40 on page 62.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). This is shown in Figure 12 on page 22. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 13 on page 23. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 14 on page 24.

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 15 on page 25. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 16 on page 26. The ^{t}DQSS (NOM) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). This is shown in Figure 17 on page 27. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until both ^{t}RAS and ^{t}RP has been met. Note that part of the row precharge time is hidden during the access of the last data elements.

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 8.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 9, which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (Figure 9 also shows the same case for ^{t}RCD; the same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 8: Activating a Specific Row in a Specific Bank

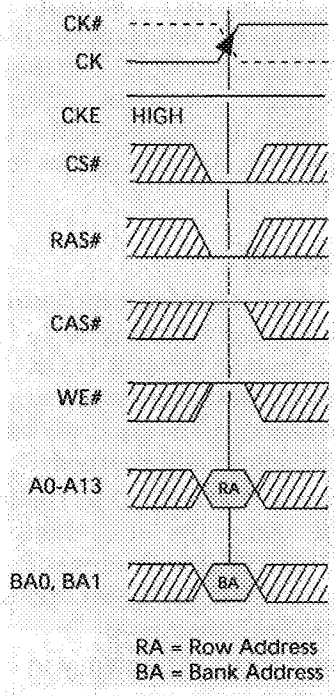
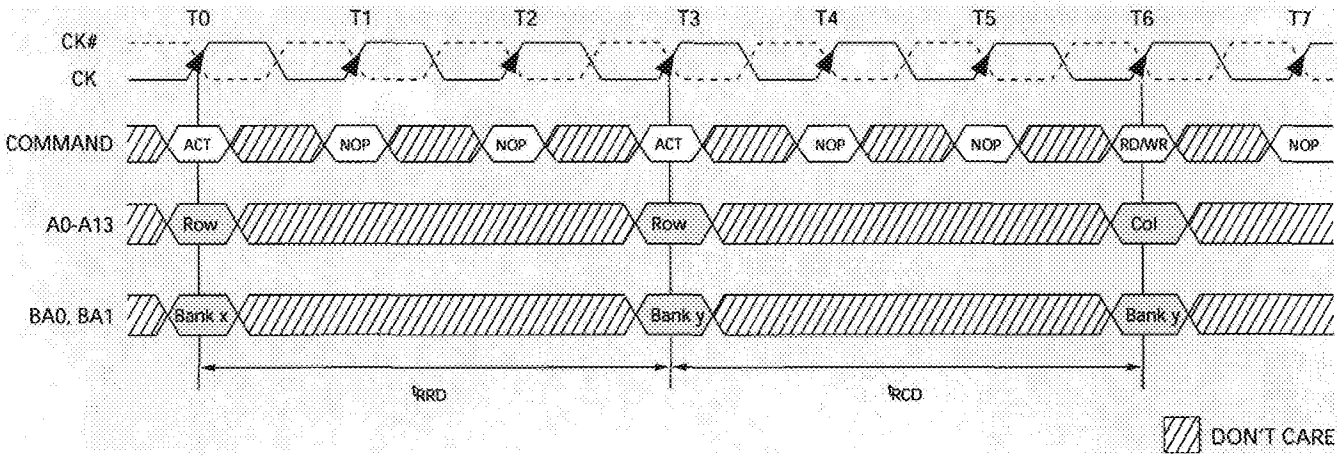


Figure 9: Example: Meeting ^{t}RCD (^{t}RRD) MIN When $2 < {}^{t}\text{RCD}$ (^{t}RRD) MIN/^{t}CK≤3



for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 1Gb DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 7.8125µs (70.3µs). Note the JEDEC specifications only allows 8 x 7.8125µs, thus the Micron specification exceeds the JEDEC requirement by one clock. This maximum absolute interval is to allow future support for DLL updates internal to the DDR SDRAM to be restricted to AUTO REFRESH cycles, without allowing excessive drift in ^{t}AC between updates.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (High) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH (A DLL reset and 200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. VREF voltage is also required for the SELF REFRESH full duration.

The procedure for exiting self refresh requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for ^{t}XSNR time, then a DLL Reset and NOPs for 200 additional clock cycles before applying any other command.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# equal HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A13. See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A13 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 9 for x16; 9, 11 for x8; or 9, 11, 12 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = 9 for x16; 9, 11 for x8; or 9, 11, 12 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described

Commands

Table 4 and Table 5 provide a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables, Table 7 on page 41, and Table 8 on page 43, appear following the Operation section, provide current state/next state information.

Table 4: Truth Table – Commands

Note 1 applies to all commands

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A13 provide the op-code to be written to the selected mode register.
3. BA0-BA1 provide bank address and A0-A13 provide row address.
4. BA0-BA1 provide bank address; A0-A*i* provide column address, (where *i*=9 for x16, *i*=9, 11 for x8, and *i*=9,11, 12 for x4) A10 HIGH enables the auto precharge feature (non persistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0-BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; for within the Self Refresh mode all inputs and I/Os are "Don't Care" except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for read bursts with auto precharge enabled and for write bursts.
9. DESELECT and NOP are functionally interchangeable.

Table 5: Truth Table – DM Operation

Note 1 applies to all commands

NAME (FUNCTION)	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

NOTE:

1. Used to mask write data; provided coincident with the corresponding data.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, and output drive strength. These functions are controlled via the bits shown in Figure 7. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

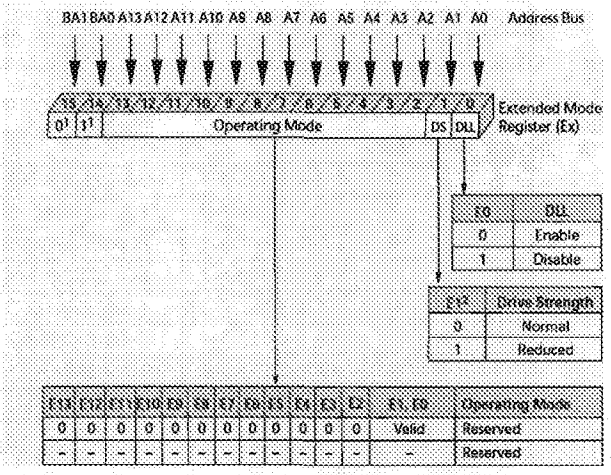
Output Drive Strength

The normal drive strength for all outputs are specified to be SSTL_2, Class II. The x16 supports a programmable option for reduced drive. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQ pins and DQS pins from SSTL_2, Class II drive strength to a reduced drive strength, which is approximately 54 percent of the SSTL_2, Class II drive strength.

DLL Enable/Disable

When the part is running without the DLL enabled, device functionality may be altered. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Figure 7: Extended Mode Register Definition



NOTE:
1. E15 and E14 (BA1 and BA0) must be "0, 1" to select the Extended Mode Register vs. the base Mode Register.
2. The reduced drive strength option is not supported on the x4 and x8 versions, and is only available on the x16 version.
3. The QFC# option is not supported.

Table 2: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS			ORDER OF ACCESSES WITHIN A BURST	
				TYPE= SEQUENTIAL	TYPE= INTERLEAVED
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

NOTE:
1. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
2. For a burst length of two, A1-A*i* select the two-data-element block; A0 selects the first access within the block.
3. For a burst length of four, A2-A*i* select the four-data-element block; A0-A1 select the first access within the block.
4. For a burst length of eight, A3-A*i* select the eight-data-element block; A0-A2 select the first access within the block.

Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, or 2.5 clocks, as shown in Figure 6.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 3 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Figure 6: CAS Latency

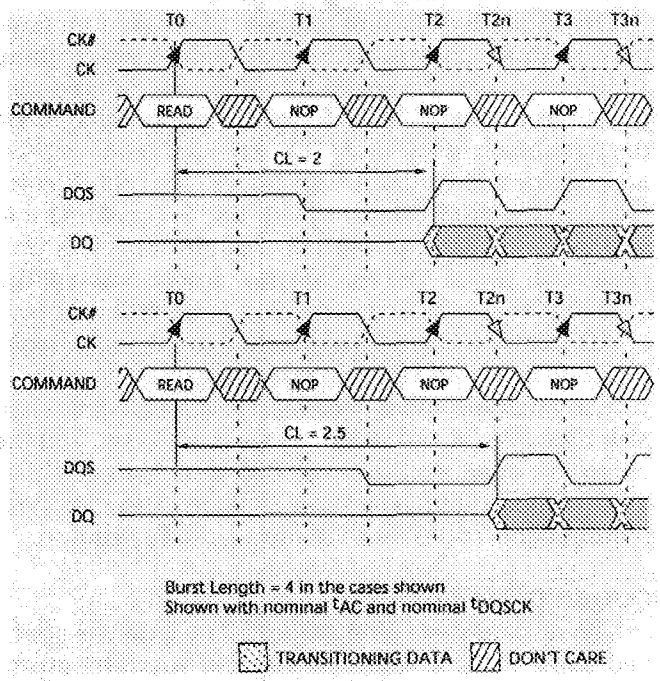


Table 3: CAS Latency (CL)

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHZ)	
	CL = 2	CL = 2.5
-75	75 ≤ f ≤ 100	75 ≤ f ≤ 133

Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A13 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A13 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A13 are reserved for future use and/or test modes. Test modes and reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 5. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

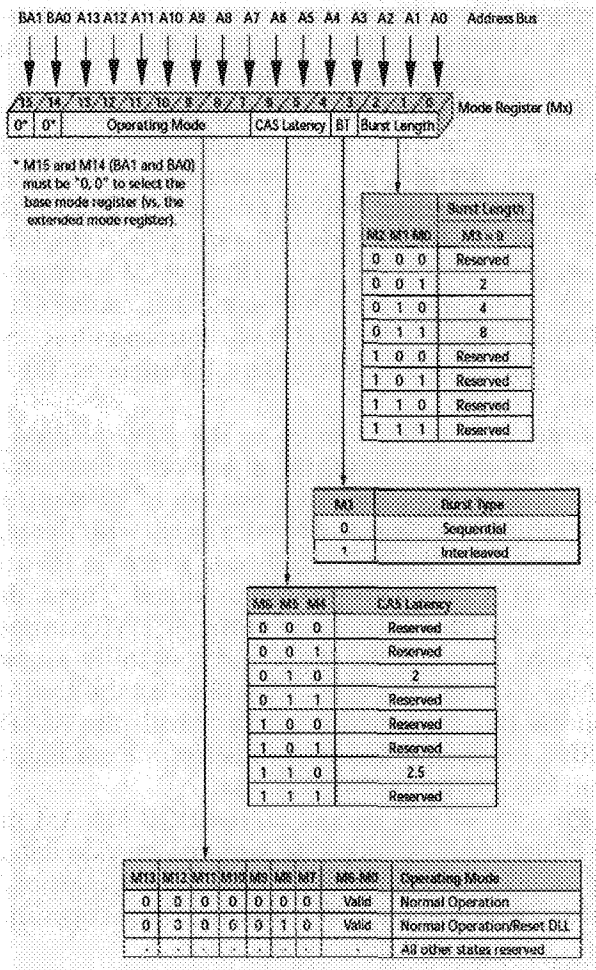
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A*i* when the burst length is set to two, by A2-A*i* when the burst length is set to four and by A3-A*i* when the burst length is set to eight (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 2, Burst Definition, on page 13.

Figure 5: Mode Register Definition



Functional Description

The 1Gb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The 1Gb DDR SDRAM is internally configured as a quad-bank DRAM.

The 1Gb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 1Gb DDR SDRAM consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A13 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to V_{DD} and V_{DDQ} simultaneously, and then to VREF (and to the system V_{TT}). V_{TT} must be applied after V_{DDQ} to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after V_{DDQ} but is expected to be nominally coincident with V_{TT}. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied. After CKE passes through V_{IH}, it will transition to a SSTL 2 signal and remain as such until power is cycled. Maintaining an LVCMOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200µs delay prior to applying an executable command.

Once the 200µs delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the extended mode register (BA1 LOW and BA0 HIGH) to enable the DLL, followed by another LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL and to program the operating parameters. Two-hundred clock cycles are required between the DLL reset and any READ command. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed (^tRFC must be satisfied.) Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) is required. Following these requirements, the DDR SDRAM is ready for normal operation.

Register Definition

Mode Register

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 5 on page 12. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A13 specify the operating mode.